Laboratoire d'Électrotechnique et d'Électronique de Puissance de Lille

Master project, 2021-2022

— Design of multi-layer PCB for efficient power conversion —

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Context

The constant growth in the demand for embedded static converters with high power density and high efficiency requires the development of new design approaches. Operating at higher frequencies (over 1 MHz) while reducing power losses are the key solutions to improve efficiency and miniaturize power converters. The advantages of Gallium nitride (GaN) power transistors in terms of electron mobility and intrinsic capacitances make them the ideal candidates for High Frequency (HF) power conversion [1]. Recent works have highlighted the benefits brought by GaN devices in designing efficient and compact power converters for various applications in domains such as automotive, aeronautics, servers… [2]-[5].

Although GaN transistors have attractive characteristics for high frequency power conversion, their switching times in the range of nanosecond causes high overvoltage and ringings due to the structural elements of the switching cells. In order to avoid a dual impact on efficiency and cooling systems of the power devices, it is necessary to reduce at its minimum the switching loop structural inductance. To achieve this goal, Printed Circuit Board (PCB) embedded power converters based on Electronic Design Automation (EDA) techniques have emerged these last years [6].

When designing power converters on PCB using bottom-side cooled GaN transistors, their thermal management can be easily improved by designing thermal vias through the FR4 substrate and optimizing their layout [7]. This method has been widely used for the PCB integration of dies [8], [9]. The recent improvements in GaN transistors packaging allow to consider applying equivalent design methods for the integration of packaged power devices in PCB assemblies. Also, it has been demonstrated that vertical switching loops can consequently reduce the total structural inductance by limiting the loop area and canceling a part of the magnetic flux [10], [11]. These results lead to lower power losses and lower Electromagnetic Interferences (EMI). However, authors in [10] have highlighted that the design of a vertical loop and thermal vias were not compatible on a single PCB.

Objective

In this context, we propose the design of a GaN-based half-bridge converter based on a mutli-layer PCB assembly. The proposed solution will allow the combination of an optimized switching loop design with an optimized thermal management for bottom-side cooled GaN transistors.

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In order to optimize the commutation loop design while offering the best thermal performances for these devices, it is proposed to separate electrical and thermal paths by achieving the multi-layer PCB assembly as shown in Fig. 1 as an example: a vertical switching loop is realized between the DC-link capacitor located on the top layer and the GaN transistors located on the intermediate layer. The heat transfer is performed from the bottom side of the GaN transistors packaging (source pad) to the bottom layer by means of thermal vias. An Aluminium Nitride (AlN) substrate is inserted between the bottom layer of the assembly and the heat sink to ensure dielectric insulation while ensuring the best thermal conductivity and spreading the heat on the heat sink area.

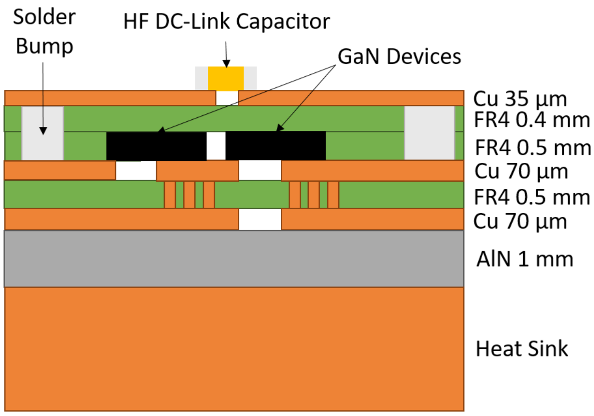

Fig. 1: Presentation of a 3-layer design half-bridge (cross-sectional view)

Work steps

Based on the the electrical design of a half bridge converter, this work will start with the design of the PCB using multiple layers. Electromagnetics simulation will emphasizes the points of attention in terms of structural inductance and the consequences on the electrical behavior. Thermal simulation will provide design rules and will confirm the effeciency of the thermal dissipation of the design.

After electromagnetic and thermal optimization thanks to simulation, the PCB will be fabricated and experimentally measured.

Some measurements could be performed to our parterned lab in Lyon (Fr.).

Keywords

Power conversion, GaN devices, PCB design, simulation, measurement, electromagnetic optimization, thermal management

References

[1] I. Omura, W. Saito, T. Domon and K. Tsuda, "Gallium Nitride power HEMT for high switching frequency power electronics," in 2007 International Workshop on Physics of Semiconductor Devices, Mumbai, India, 16-20 Dec. 2007 .

[2] X. Zhou, B. Sheng, W. Liu, Y. Chen, L. Wang, Y.-F. Liu and P. C. Sen, "A High-Efficiency High-Power-Density On-Board Low-Voltage DC–DC Converter for Electric Vehicles Application," IEEE Transactions on Power Electronics, vol. 36, no. 11, pp. 12781 - 12794, Nov. 2021.

[3] M. Schiestl, F. Marcolini, M. Incurvati, F. G. Capponi, R. Stärz, F. Caricchi, A. S. Rodríguez and L. Wild, "Development of a High Power Density Drive System for Unmanned Aerial Vehicles," IEEE Transactions on Power Electronics, vol. 36, no. 3, pp. 3159 - 3171, March 2021.

[4] M. H. Ahmed, M. A. d. Rooij and J. Wang, "High-Power Density, 900-W LLC Converters for Servers Using GaN FETs: Toward Greater Efficiency and Power Density in 48 V to 6V/12 V Converters," IEEE Power Electronics Magazine, vol. 6, no. 1, pp. 40 - 47, March 2019.

[5] F. Salomez, S. Vienot, B. Zaidi, A. Videt, T. Duquesne, H. Pichon, E. Semail and N. Idir, "Design of an integrated GaN inverter into a multiphase PMSM," in 2020 IEEE Vehicle Power and Propulsion Conference (VPPC), Gijon, Spain, 18 Nov.-16 Dec. 2020.

[6] C. Buttay, C. Martin, F. Morel, R. Caillaud, J. L. Leslé, R. Mrad, N. Degrenne and S. Mollov, "Application of the PCB-Embedding Technology in Power Electronics – State of the Art and Proposed Development," in 2018 Second International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), College Park, MD, USA, 25-27 June 2018.

[7] S. Zhang, E. Laboure, D. Labrousse and S. Lefebvre, "Thermal management for GaN power devices mounted on PCB substrates," in 2017 IEEE International Workshop On Integrated Power Packaging (IWIPP), Delft, Netherlands, 5-7 April 2017.

[8] S. Moench, R. Reiner, P. Waltereit and a. al., "PCB-Embedded GaN-on-Si Half-Bridge and Driver ICs With On-Package Gate and DC-Link Capacitors," IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 83 - 86, Jan. 2021.

[9] B. Weiss, R. Reiner, P. Waltereit, R. Quay and O. Ambacher, "Operation of PCB-embedded, high-voltage multilevel-converter GaN-IC," in 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, USA, 30 Oct.-1 Nov. 2017.

[10] B. Sun, K. L. Jørgensen, Z. Zhang and M. A. Andersen, "Research of Power Loop Layout and Parasitic Inductance in GaN Transistor Implementation," IEEE Transactions on Industry Applications, vol. 57, no. 2, pp. 1677 - 1687, March-April 2021.

[11] L. Pace, N. Idir, T. Duquesne and J.-C. D. Jaeger, "Parasitic loop inductances reduction in the PCB layout in GaN-based power converters using S-parameters and EM simulations," Energies, vol. 14, no. 5, p. 1495, March 2021.