Master project, 2024-2025

Improvement of PCB Layout for Fast-Switching Power Converters

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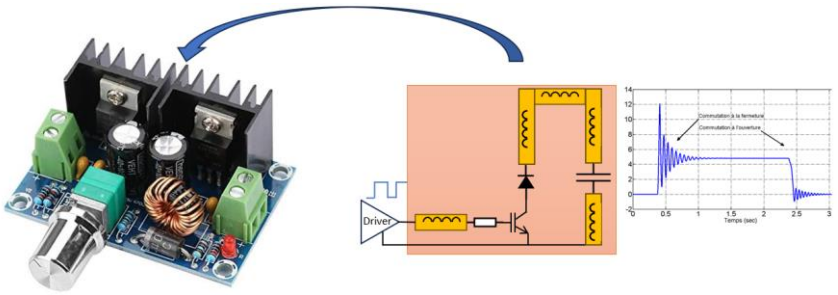
Context

Power electronic converters are crucial for managing electrical energy in a variety of applications, from household electronics to high-power industrial systems [1]. As the demand for higher efficiency and compact designs increases, the switching frequency of converters is being pushed higher notably for embedded systems [2],[3]. However, this brings to significant challenges, such as the emergence of parasitic effects in printed circuit boards (PCBs) that can degrade the performance of switching cells [4],[5]. This project aims to study these parasitic inductances in PCBs and their impact on the performance of high-frequency switching cells, with the goal of enhancing their efficiency.

At the **Power Electronics group** in L2EP laboratory, extensive research has been conducted on the impact of parasitic inductance effects in high-frequency power converters, and also proposing methods to reduce these effects [5], [6]. Recent works have also demonstrated that mutual coupling between power and control loops can lead to significant disturbances in circuit performance, causing issues such as increased electromagnetic emissions and thermal losses [7].



Objectives

The main objective of this project is to investigate and characterize the parasitic inductances present in the power and control loops of PCBs used in high-frequency switching cells. The research will also include an analysis of the mutual coupling between these loops and its impact on circuit performance. Advanced simulation tools such as ADS electromagnetic (EM) simulation will be used to model these parasitic elements. Experimental validation will be conducted using high-precision measurement equipment, including oscilloscope and impedance analyzer, to compare with the simulation results. Based on this study, the project aims to propose an optimized PCB design strategy to minimize the effects of parasitic inductances.

Schedule

The project will start with a comprehensive review of the literature on PCB parasitic effects and mutual coupling phenomena, followed by initial simulation work to model the parasitic inductances in the PCB of power and control loops. This will be validated by experimental measurements of parasitic inductances and mutual coupling effects using dedicated test benches (oscilloscope, VNA). The second phase of the project will focus on refining the simulation models based on experimental data. By the end of the project, the candidate will propose an optimization method bases on this study in order to minimize the parasitic effects in high-frequency switching applications.

Application Process

Candidates interested in this project should contact email addresses with a CV and their latest academic transcripts. Shortlisted candidates will be invited for an interview to discuss the project details and their fit for the research. The internship will take place at the ESPRIT building of the University of Lille, where the candidate will have access to state-of-the-art simulation and measurement tools to carry out this work.

References

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