

Master project, 2025-2026

Design and realization of overcurrent-resistant chip packages

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Context

The energy sector is currently experiencing a revolution thanks to the increasing share of renewable energies on the grid production. However, those sources of energy produce a voltage which is not adapted to the existing grid, making the use of power electronics mandatory. On its side, power electronics is also experiencing a revolution, made this time possible by the launch of new "wideband gap" SiC and GaN components on the market with much better characteristics than Si components (Figure 1a). These new components represent a major opportunity for power electronics, even if their full use is still limited by a number of obstacles.

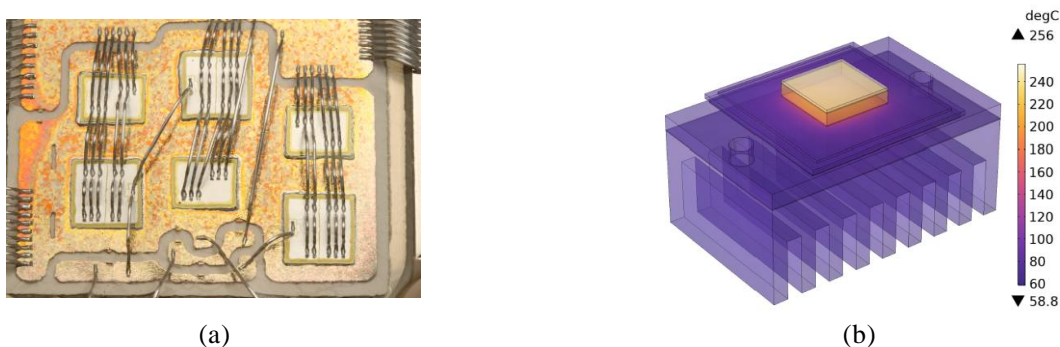


Figure 1: (a) Power electronics layout with Si chips; (b) Thermal simulation of basic assembly in power electronics [1]

When it comes to injecting power into the grid, the main obstacle is the lack of resilience that these components have when they need to deal with grid current surge [1]. In fact, protection circuits present on the grid generally have response times which are longer than the time required for overcurrent to destroy the component. For this reason, one of the key priority of the power electronics sector is to develop a solution to make SiC and GaN components much more resilient to overcurrent. One of the objectives of the L2EP and G2Elab laboratories is to develop innovative packages to find a solution to this challenge.

Objectives

The aim of this research project is to develop and characterize power electronics assemblies with attractive thermal impedances regarding overcurrent.

First, the trainee will conduct a literature review on the various methods of measuring junction temperature in power electronics. Next, using an existing test bench, the trainee will compare two temperature measurement methods: one based on measuring the thermosensitive coefficient and the other based on optical measurement. Finally, once the two methods have been validated on standard samples produced by the trainee, samples with thermal impedance that is useful for managing overcurrents will need to be produced and tested.

Candidate and location

The ideal candidate will have a degree in electrical engineering (Master degree), knowledge of thermal engineering will be appreciated. Interested candidates should send their CV to the above e-mail address to arrange an interview. Latest transcripts must be provided. The possibility of a PhD following the internship may be considered. The internship will take place in the ESPRIT building of the University of Lille within the Power Electronics team of the L2EP laboratory. The internship will be co-supervised by the G2Elab laboratory in Grenoble.

References

- [1] S. Bhadoria, S. G S and H. -P. Nee, "Comparison of Top and Bottom Cooling for Short Duration of Over-Currents for SiC Devices: An Analysis of the Quantity and Location of Heat-Absorbing Materials," in *IEEE Open Journal of Power Electronics*, vol. 5, pp. 765-778, 2024, doi: 10.1109/OJPEL.2024.3407163.