LABORATOIRE D'ELECTROTECHNIQUE ET D'ELECTRONIQUE DE PUISSANCE DE LILLE

Master thesis, 2026-2027

Design, modelling and validation of the PCB of a GaN-based converter

Supervisor : Issa ALAJI (L2EP, Université de Lille)

Contact: issa.alaji@univ-lille.fr

Context

Power converters are increasingly built around wide-bandgap devices, SiC and GaN, which switch far faster than their silicon counterparts [Millan 2014]. The aim is to raise the switching frequency: for a given ripple the passives and filters shrink, so power density increases [Yuan 2021].

This speed comes at a cost. The dv/dt reaches several tens of V/ns, so the spectral content extends to a few hundred MHz, well beyond the switching frequency. In this range the PCB parasitics - power and gate loop inductances and their mutual - set the overvoltage, the ringing and the EMI [Reusch 2014]; minimizing them has become a first-order layout constraint [Wang 2017]. Electromagnetic (EM) simulation quantifies them accurately but is computationally costly. Equivalent circuits of PCBs - using lumped elements- identified from the S/Z matrices are a practical alternative, whose experimental validation remains far less documented than the extraction itself.

This internship is part of a GDR SEEDS project, an L2EP - GREMAN collaboration on a GaN converter, whose full chain is: PCB design → EM extraction → equivalent circuit (fitting) → SPICE simulation → manufacturing → measurements. This internship is restricted to the PCB stage: layout, EM simulation providing the S/Z matrices used for the fitting, and experimental validation by VNA.

Objective

Design the PCB of a GaN buck converter with minimized parasitics, extract its S/Z matrices by EM simulation for the identification of an equivalent circuit, and validate this extraction by VNA measurement.

Work plan. (1) Design of the buck PCB (GaN half-bridge, gate driver, decoupling) with minimized power and gate loops. (2) Multiport EM simulation, ports at the component footprints: S/Z matrices transmitted to the partner (GREMAN) for the fitting. (3) Two-port EM simulation with short-circuited footprints, targeting the power and gate loop inductances and their mutual. (4) VNA validation: 0 Ω bridges reproducing the previous configuration, SMA connectors, measurement, de-embedding, comparison with simulation; the residual inductance of the bridges and connectors is to be quantified.

Expected results: a PCB with reduced parasitics; the multiport S/Z matrices transmitted to GREMAN; the experimental validation of the EM extraction with a quantified simulation/measurement deviation.

Key words

GaN converter, PCB layout, parasitic inductance, electromagnetic simulation, S/Z parameters, equivalent circuit model, VNA measurement, de-embedding, EMC/EMI.

References

[Millan 2014] J. Millán et al., "A survey of wide bandgap power semiconductor devices", IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2155–2163, 2014.

[Yuan 2021] X. Yuan, I. Laird, S. Walder, "Opportunities, challenges and potential solutions in the application of fast-switching SiC power devices and converters", IEEE Trans. Power Electron., vol. 36, no. 4, pp. 3925–3945, 2021.

[Reusch 2014] D. Reusch, J. Strydom, "Understanding the effect of PCB layout on circuit performance in a high-frequency gallium-nitride-based point of load converter", IEEE Trans. Power Electron., vol. 29, no. 4, pp. 2008–2015, 2014.

[Wang 2017] K. Wang et al., "A multiloop method for minimization of parasitic inductance in GaN-based high-frequency DC–DC converter", IEEE Trans. Power Electron., vol. 32, no. 6, pp. 4728–4740, 2017.