



- PhD position -Grid codes for MVAC/MVDC interface Université Paris-Saclay & Centrale Lille

Supervisors:

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Dates: September/December 2023 - September/December 2026 (36 months)

Keywords: DC electric grid, power electronics

Program PEPR Tase DC ArchitectTec.1.1 : Architectures des réseaux et électronique de puissance WP 1: Architectures and operation of hybrid AC and DC distribution Task 1.2: Technical connection and operational constraints: Towards DC grid codes PhD 1: Technical constraints for PEC to operate within the grids' architectures

I – Research proposal

Title: Grid codes for MVAC/MVDC interface

Introduction

At the interface between the MVAC electric grid and the future MVDC electric grid, power electronics converters play a major role. Their primary function is to ensure AC/DC conversion and power flow control. But they could also provide auxiliary functions to improve the operation of hybrid AC and DC grids:

- in steady state, the converters could provide system services for the AC and/or DC grid such as reactive power supply or DC pole voltage balancing.
- in fault conditions, the converters could participate in the detection of the fault and its cut-off. The solution will have to respect the selectivity of the network, but also ensure the resilience of the converter.

In addition, in the event of a failure of one of the converter components, continuity of operation must also be ensured. The topology, the dimensioning and thus the cost of an interface converter depend strongly on the desired auxiliary functions. The impact is currently difficult to estimate.

Challenges

The problem addressed by this thesis can be summarized as follows: Which specifications for the interface between the MVAC grid and the future MVDC grid?

This thesis will link the desired operating modes of the MVDC networks (WP 1 Task 1) and the constraints that this imposes on the converters (WP 2). The deliverable will take the form of specifications for converters at the interface of MVAC and MVDC grids, in terms of operation and performance, protection (selectivity, resilience), and AC and DC system services. They could be considered as initial contributions to a grid code for MVDC electric grids. The realization of a suitable power converter prototype could be envisaged.

References

[1] Commission Regulation (EU) 2016/1447 of 26 August 2016 establishing a network code on requirements for grid connection of high voltage direct current systems and direct current-connected power park modules (Text with EEA relevance), https://eur-lex.europa.eu/eli/reg/2016/1447/oj

[2] CENELEC (Comité européen de normalisation en électronique et en électrotechnique), HVDC Grid Systems and connected Converter Stations - Guideline and Parameter Lists for Functional Specifications - Part 1: Guidelines, https://standards.iteh.ai/catalog/standards/clc/31afd1e2-faed-44a4-a7ee-d938f6cae664/clc-ts-50654-1-2020

II - Scientific environment

The position offered is a PhD in co-supervision between the GeePs of Université Paris-Saclay and the L2EP of Centrale Lille. Strong background is available in electric power grids and power electronics.

The doctoral student will work in the GeePs laboratory, in the Bréguet building of CentraleSupélec, at Gif-sur-Yvette. He will visit regularly the L2EP in Centrale Lille. He will have access to the experimental room of the GeePs' HVDC group, which includes the equipment necessary for the prototyping of power electronics converters. He will also have access to the equipment of the GeePs Power electronics group, the GeePs support workshops and the CentraleSupélec FabLab.

III – Candidate profile

Eligible candidates should have a Master degree at the power grid-power electronics interface. We seek for a highly motivated candidate that would preferably have some background in power electronics prototyping. Experience in power grid simulation would be an advantage.

IV – Contract

The position will open in September 2023 (flexible starting date). The contract is for 3 years. The salary will be defined according to University Paris-Saclay rules regarding doctoral student remuneration. The work will be performed at GeePs CentraleSupélec, in GeePs installations.

V – Contact

Please send a CV and a motivation letter to: Jing DAI, GeePs, CentraleSupélec, Université Paris-Saclay, e-mail: jing.da@centralesupelec.fr Ferréol BINOT, L2EP, Centrale Lille, e-mail: ferreol.binot@centralelille.fr