A Novel Space-Vector Current Control Based on Circular Hysteresis Areas of a Three-Phase Neutral-Point-Clamped Inverter

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***Abstract*—This paper presents a novel space-vector current-control strategy for three-phase neutral-point (NP)-clamped inverters. The main task of this control technique is to force the actual current vector to reach the reference current vector. This original strategy consists in defining three circular hysteresis bands around the error vector. Then, according to the location of this error vector, a selection process of the next applied vector is used to minimize the error vector. The NP voltage is balanced by using the redundant inverter switching states. Simple lookup tables are required for area and sector detection, as well as for vector selection. The performance of the proposed control technique is demonstrated through simulation and experimental investigations.**

***Index Terms*—Circular hysteresis areas, neutral-point (NP) voltage control, space-vector current control (SVCC), three-phase neutral-point-clamped (NPC) inverter.**

I. Introduction

MULTILEVEL inverters [1], [2] are becoming an established means for developing new high-power applications requiring significant increase of both current and voltage magnitudes. The advantages of multilevel inverter are well known since the first neutral-point-clamped (NPC) inverter was proposed in 1981 by Nabae *et al.* [3]. The particular topology of multilevel inverters increases the power rating since the blocking voltage of each switch is one-half of the dc-link voltage [4]–[7]. Furthermore, their output-voltage harmonic content is much smaller than that of two-level inverters with the same switching frequency because of the output-voltage waveform improvements [8].

Many control strategies for multilevel inverters have been proposed to control either voltages [9]–[14] or currents [15]–[18]. They can be classified mainly into two categories: indirect current control techniques and direct current (dc) control techniques.

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Carrier-based modulation (CBM) and space-vector modulation (SVM) belong to the first category. They have been considered as among the most popular modulation strategies for multilevel inverters due to their operation at fixed frequency. However, the CBM method controls each line current separately using a linear controller and a comparison between a triangular carrier and a phase reference signal. Hence, a complex analog circuit is required. Nevertheless, devices have to be added to the CBM to balance the dc-link voltage.

In contrast to the CBM, the SVM strategy controls the three-phase voltages by using a single space-vector reference and can also balance the dc-link voltage by using the redundant inverter switching states [24], [25]. The SVM scheme is based on the application of a zero vector and the three nearest voltage vectors. Thus, multiple timers are needed for calculating the four duty cycles. Moreover, the complexity of involved calculations requires a powerful microprocessor or DSP. These strategies are generally used with a proportional–integral regulator or a deadbeat regulation strategy to control the three-phase currents [19].

An alternative approach to regulate the current through multilevel inverters is to use a direct control of the currents. To determine the switching instants for each inverter leg, three independent hysteresis comparators are the simplest implementation. Furthermore, this simple hardware current-control system does not require any knowledge of load parameters. However, it suffers from a high-frequency operation as well as line-current interactions [20], and the balancing of the neutral-point (NP) voltage of the multilevel inverters is difficult to achieve.

In this paper, a space-vector current control (SVCC) is investigated in order to use circular hysteresis areas and to perform the balancing of the dc bus voltages. The proposed SVCC gathers the three error currents into a single space-vector quantity. In this case, the error-vector tip moves on three areas limited by two circular contours. The control scheme is based on the detection of the area and the sector in which the vector tip of the current error can be located. Then, an appropriate voltage vector among the 27 voltage vectors of the NPC inverter will be applied to force the current error back toward the hysteresis boundaries and, at the same time, to control the NP voltage through the use of the redundant inverter switching states. Simple lookup tables are required for the area and sector detection, as well as for the vector selection. The proposed

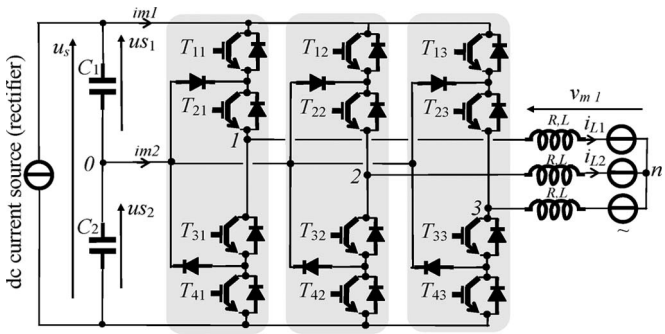

Fig. 1. Structure of the NPC inverter.

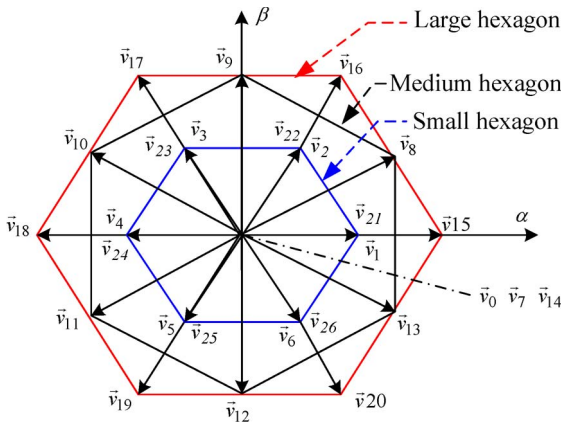

Fig. 2. Three-level voltage inverter vectors in the $\alpha\beta$ frame.

control technique has been verified through simulations and experimental tests.

II. Power-Circuit Structure

The NPC inverter structure consists of three vertical commutation circuits, which are fed from a capacitive voltage divider (Fig. 1). Each commutation circuit is made up of four switches. Additional steering diodes are required to clamp one terminal of each transistor to the capacitor midpoint. The voltage across each capacitor must be maintained equal to half the value of the full dc voltage (u_s) to ensure good operation of the NPC inverter

$$u_{s1} = u_{s2} = \frac{u_s}{2}. \tag{1}$$

The 27 switching states of the NPC inverter result in 27 voltage vectors. Among these vectors, three are zero voltage vectors $(\vec{v}_0, \vec{v}_7,$ and $\vec{v}_{14})$ and 24 are nonzero voltage vectors. By drawing these 27 voltage vectors in the $\alpha\beta$ frame, three hexagons are distinguished (large, medium, and small) as illustrated in Fig. 2.

III. CHCC

In contrast to a classical hysteresis control for a conventional two-level inverter, the conventional hysteresis current control (CHCC) for a three-level inverter applies three voltage levels $(+u_s/2,\ -u_s/2,$ and 0) to each phase instead of two. The voltage levels are calculated by taking into account the current

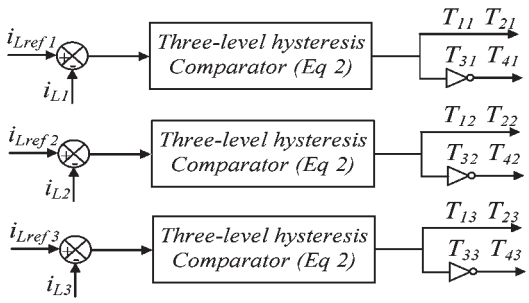

Fig. 3. CHCC principle.

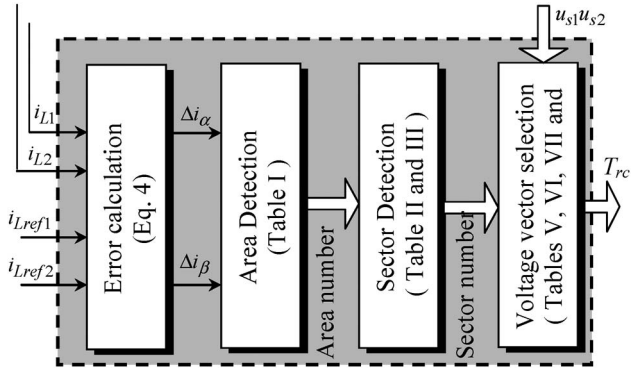

Fig. 4. General scheme SVCC.

error value $\Delta i = i_{L\text{ref}} - i_L$ and two hysteresis bands h_1 and h_2 (upper and lower hysteresis bands) (Fig. 3)

$$v = \begin{cases} -u_s/2, & \text{if } \Delta i > h_2 \\ 0, & \text{if } (h_1 < \Delta i < h_2) \text{ or } (-h_2 < \Delta i < -h_1) \\ +u_s/2, & \text{if } \Delta i < -h_2. \end{cases} \tag{2}$$

The CHCC provides a fast and accurate response without any knowledge of load parameters. However, the switching frequency may vary widely during the fundamental period, resulting in irregular inverter operation. This is mainly due to the interference between the three-phase commutations since each line current not only depends on the corresponding phase voltage but is also affected by other voltages.

IV. Proposed SVCC Scheme

A. General Control Scheme

In order to ensure the correct multilevel operation, the control system has to fulfill two tasks. It must generate the correct voltage vector and hence, the correct multilevel waveform. At the same time, it must maintain the same voltage across the two capacitors (Fig. 1).

Fig. 4 illustrates the general control scheme of the NPC inverter. The proposed SVCC consists of four blocks: error calculation, area detection, sector detection, and voltage-vector selection.

B. Area Detection

The goal of the proposed SVCC is to keep the actual load current close to the reference load current within the hysteresis

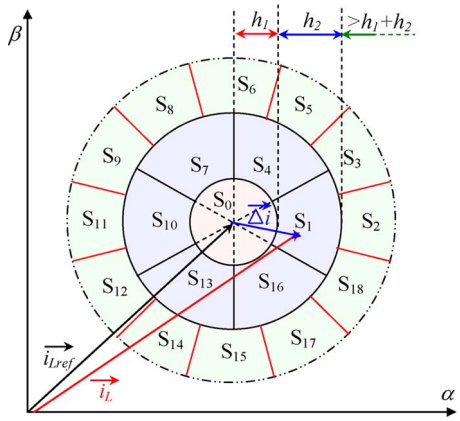

Fig. 5. Error-vector tip location in the 19 sectors with hysteresis areas.

boundaries. For the three-phase balancing sinusoidal currents, the tip of the reference current vector moves on a circle around the origin of the coordinate system. The analysis of the system is performed in the transformed $(\alpha\beta)$ frame, and the transformation of the three hysteresis bands into this frame results in three circular areas as shown in Fig. 5.

Three hysteresis bands are chosen in order to use four categories of available voltage vectors, which are zero, small, medium, and large. This organization makes possible the selection of an appropriate voltage vector, and the strategy will be detailed in Section IV-D. The first area $A_{\rm I}$ is defined as the surface surrounded by the circle with radius h_1.

The second area $A_{\rm II}$ is defined as the surface delimited by the two circles with radii h_1 and $h_1 + h_2$, respectively. The third area $A_{\rm III}$ is the area outside the circle of radius $h_1 + h_2$.

The values of the h_1 and h_2 radii depend on the value of the current reference and on the desired control dynamics. The choice $h_1 = 0$ may increase the switching frequency since no zero voltage vectors are used. In addition, this choice enables a fast response of the load current control. The radius h_2 must be different from zero $(h_2 \neq 0, h_2 > h_1 > 0)$ to allow the NP voltage balancing through the use of redundant space vectors (Section IV-E).

The reference load current $i_{L\_\rm ref}$ and the actual load current i_L can be expressed by using vector components in a complex form

$$\begin{cases} \bar{i}_{L\rm ref} = i_{L\rm ref\alpha} + j i_{L\rm ref\beta} \\ \bar{i}_L = i_{L\alpha} + j i_{L\beta}. \end{cases} \tag{3}$$

Similarly, the error vector is defined by

$$\bar{\Delta} i = \bar{i}_L - \bar{i}_{L\rm ref}. \tag{4}$$

It is expressed in the $\alpha\beta$ reference frame as

$$\bar{\Delta} i = \Delta i_\alpha + j \Delta i_\beta. \tag{5}$$

The tip of the reference current vector $\vec{i}_{L\_\rm ref}$ is located in the center of area $A_{\rm I}$ (Fig. 5). The tip of the actual current vector $\vec{i}_L$ can be located in one of the three areas $A_{\rm I}$, $A_{\rm II}$, or $A_{\rm III}$, delimited by the two circles $r = h_1$ and $r = h_1 + h_2$. Table I summarizes the conditions that must be satisfied for the error vector $\overline{\Delta} i$ to be located in each particular area.

TABLE I
AREAS AND CORRESPONDING $\overline{\Delta} i$ CONDITIONS

Conditions	Areas
$\left\|\overline{\Delta i}\right\| = \sqrt{\Delta i_\alpha^2 + \Delta i_\beta^2} < h_1$	$A_{\rm I}$
$h_1 < \left\|\overline{\Delta i}\right\| = \sqrt{\Delta i_\alpha^2 + \Delta i_\beta^2} < h_1 + h_2$	$A_{\rm II}$
$\left\|\overline{\Delta i}\right\| = \sqrt{\Delta i_\alpha^2 + \Delta i_\beta^2} > h_1 + h_2$	$A_{\rm III}$

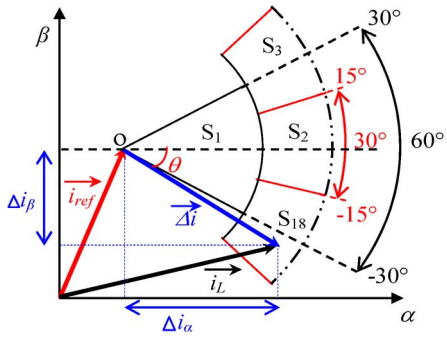

Fig. 6. Angles between two adjacent sectors.

C. Sector Detection

As shown in Fig. 5, areas $A_{\rm I}$ and $A_{\rm II}$ are bounded by the hysteresis boundaries h_1 and $(h_1 + h_2)$, respectively, whereas area $A_{\rm III}$ has no upper limit $(r > h_1 + h_2)$.

Area $A_{\rm I}$ represents one sector, which is S_0. Area $A_{\rm II}$ is subdivided into six sectors: S_1, S_4, S_7, S_{10}, S_{13}, and S_{16}. As shown in Fig. 6, the angle between any two consecutive sectors is 60°. For instance, sector $S_1$is located between $-30°$ and 30°.

Area $A_{\rm III}$ is subdivided into 12 sectors that are S_2, S_3, S_5, S_6, S_8, S_9, S_{11}, S_{12}, S_{14}, S_{15}, S_{17}, and S_{18}. Fig. 6 shows that the angle between adjacent sectors is 30°. For example, sector S_2 lies between $-15°$ and 15°.

The detection of the sector in which the tip of the current-error vector sits is made according to the following two conditions:

1) the area to which it pertains;
2) the angle θ between the error vector $\Delta\vec{i}$ and the parallel to the α axis.

As illustrated in Fig. 6, the angle θ is defined by the following expression:

$$\theta = \arctan\left(\frac{\Delta i_\beta}{\Delta i_\alpha}\right). \tag{6}$$

The error-vector tip can be located in any of the 19 sectors depending on the value of the angle θ and the area number. Except for area $A_{\rm I}$, which represents a single sector S_0, Tables II and III give the conditions that must be satisfied for the error vector $\overline{\Delta} i$ to belong to each particular sector.

D. Voltage-Vector Selection

When the error-vector tip is located in area $A_{\rm I}$ (sector S_0), the error is small and is considered acceptable within the required accuracy for the tracking of the current references.

TABLE II
DEFINITION OF AREA A_{II} SECTORS

Angle θ	Sector
-30° < θ < 30°	S_1
30° < θ < 90°	S_4
90° < θ < 150°	S_7
150° < θ < 210°	S_{10}
210° < θ < 270°	S_{13}
270° < θ < 330°	S_{16}

TABLE III
DEFINITION OF AREA A_{III} SECTORS

Angle θ	Sector
-15° < θ < 15°	S_2
15° < θ < 45°	S_3
45° < θ < 75°	S_5
75° < θ < 105°	S_6
105° < θ < 135°	S_8
135° < θ < 165°	S_9
165° < θ < 195°	S_{11}
195° < θ < 225°	S_{12}
225° < θ < 255°	S_{14}
255° < θ < 285°	S_{15}
285° < θ < 315°	S_{17}
315° < θ < 345°	S_{18}

Then, one of the three zero voltage vectors ($\vec{v}_0, \vec{v}_7,$ and $\vec{v}_{14}$) is applied, and no connection is used [Fig. 7(a)].

In the same way, one of the small hexagon voltage vectors will be applied if the error-vector tip is located in area A_{II} [Fig. 7(b)].

For the third area A_{III}, if the error-vector tip is located in any of sectors S_3, S_6, S_9, S_{12}, S_{15}, or S_{18}, one of the medium hexagon voltage vectors will be selected [Fig. 7(c)]. Otherwise, one of the large hexagon voltage vectors will be applied when the error-vector tip is located in one of the following sectors: S_2, S_5, S_8, S_{11}, S_{14}, or S_{17} [Fig. 7(d)].

To understand the selection rule of the appropriate voltage vector, we will consider a sector from each area (Fig. 7).

If the error-vector tip is located in sector S_1 of area A_{II} [Fig. 7(b)], the appropriate voltage vector to move the error back toward the hysteresis area A_{I} is either $\vec{v}_4$ or $\vec{v}_{24}$. The choice between $\vec{v}_4$ and $\vec{v}_{24}$ is made according to the sign of the NP voltage $\Delta u_s = u_{s1} - u_{s2}$ (this process is explained in Section IV-E).

If the error-vector tip is located in sector S_3 of area A_{III} [Fig. 7(c)], the best choice to get back the error toward the hysteresis area A_{II} is $\vec{v}_{11}$.

If the error-vector tip is located in sector S_2 of area A_{III} [Fig. 7(d)], $\vec{v}_{18}$ is the suitable voltage vector to get back the error toward the hysteresis area A_{II}.

The current-error sectors of area A_{II} are shifted 30° from the voltage sectors of the small hexagon [Fig. 7(b)]. In the same way, the current-error sectors S_3, S_6, S_9, S_{12}, S_{15}, and S_{18} of area A_{III} are shifted 15° with respect to the voltage sectors of the medium hexagon [Fig. 7(c)]. Likewise, the current-error sectors S_2, S_5, S_8, S_{11}, S_{14}, and S_{17} of area A_{III} are shifted 15° with respect to the voltage sectors of the large hexagon [Fig. 7(d)]. This choice is made to allow a good operation of the NPC inverter owing to a better selection of the voltage vectors.

To understand better the selection process, we consider the case where the error-vector tip is located in sector S_1 (Fig. 8). In this case, the appropriate voltage vector to apply is either $\vec{v}_4(011)$ or $v_{24}(-100)$. The next applied voltage vector is as follows:

1) $\vec{v}_{18}(-111)$ if the error-vector tip moves toward S_2;
2) $\vec{v}_{11}(-101)$ if the error-vector tip moves toward S_3;
3) $\vec{v}_{10}(-110)$ if the error-vector tip moves toward S_{18};
4) $\vec{v}_5(001)$ or $\vec{v}_{25}(-1-10)$ if the error-vector tip moves toward S_4;
5) $\vec{v}_3(-110)$ or $\vec{v}_{23}(-10-1)$ if the error-vector tip moves toward S_{16};
6) $\vec{v}_0(000)$ or $\vec{v}_7(111)$ or $\vec{v}_{14}(-1-1-1)$ if the error-vector tip moves toward S_0.

In all these cases, it is clear that the selected voltage vector ensures a correct multilevel waveform (the switching voltages u_{10}, u_{20}, and u_{30} do not jump levels).

E. NP Voltage Control

The unbalance of the NP voltage problem [21], [22] can be solved by using two external dc regulated voltage sources. It can be solved also by using voltage regulators for each capacitor voltage with the help of a controlled multilevel rectifier [23] or by modifying pulsewidth-modulation patterns and voltage-vector selections [24], [25]. With the proposed control strategy, the NP voltage can be easily controlled by applying appropriate voltage vectors. The 27 voltage vectors are divided into three categories according to their magnitudes: large, medium, and small Fig. 2). Each of the three categories affects the charge balance in a different way.

The large vectors have no effect on the NP voltage. The medium vectors connect one of the line currents to the NP, but their effect is not controllable since they have only one realization. The small vectors connect one or two line currents to the NP. In addition, they have two realizations: one positive and one negative switching pattern.

The positive switching pattern charges the upper capacitor C_1, whereas the negative one discharges it. Table IV illustrates the NP current i_{m2} and the charging state of the capacitor C_1 for the switching combinations of different small vectors. It is clear that vectors ($\vec{v}_1, \vec{v}_2, \vec{v}_3, \vec{v}_4, \vec{v}_5,$ and $\vec{v}_6$) generate a negative NP current that discharges the C_1 capacitor.

Similarly, vectors ($\vec{v}_{21}, \vec{v}_{22}, \vec{v}_{23}, \vec{v}_{24}, \vec{v}_{25},$ and $\vec{v}_{26}$) generate a positive NP current that charges the same capacitor.

The selection of the appropriate voltage vector must satisfy both the following conditions:

1) the control of the load currents with the proposed SVCC;
2) the control of the NP voltage by using the redundant inverter switching states.

Fig. 9 shows the control algorithm of the SVCC including the NP voltage-control part. The highlighted part of this algorithm, which is responsible of the NP voltage control, is involved only when the vector tip of the current error $\Delta\vec{i}$ is located in the area A_{II}.

Tables V–VIII display the switching tables for each sector in areas A_{I}, A_{II}, and A_{III}. Tables VI and VII show the switching tables for each sector in area A_{II} in the cases where the upper capacitor C_1 discharges and charges, respectively.

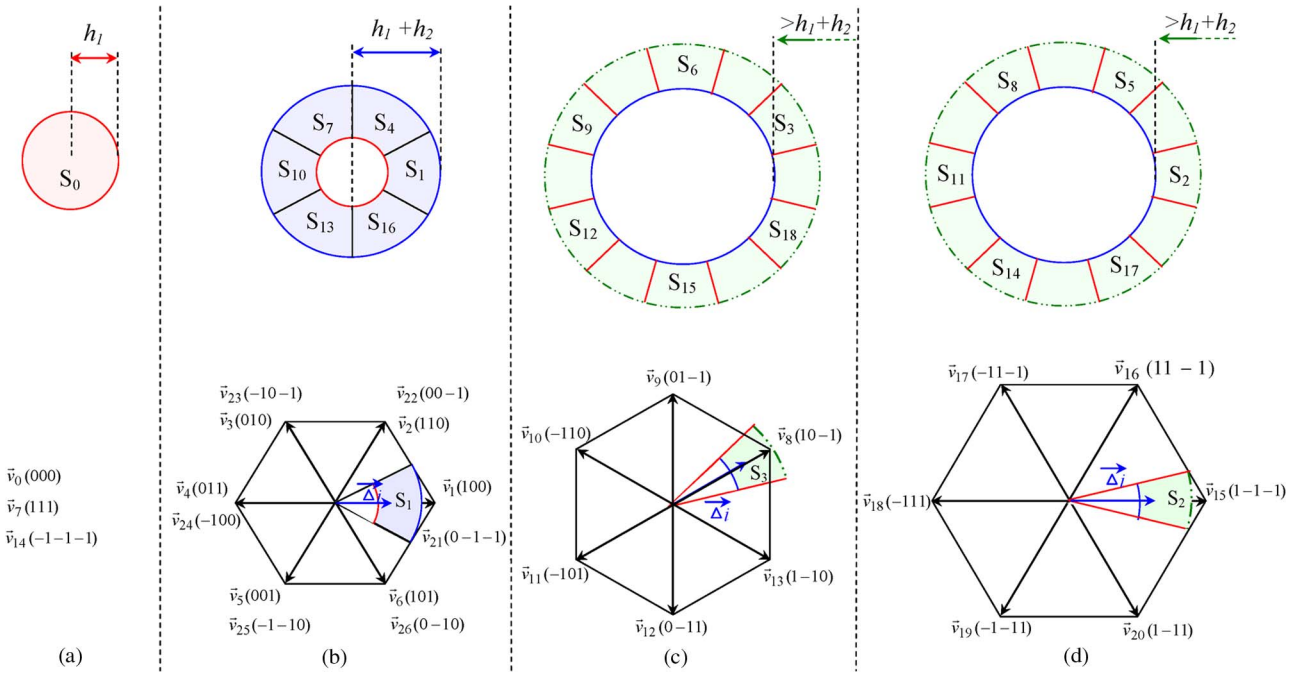

Fig. 7. Error-vector tip location and corresponding selected voltage vector category. (a) Area A_{I}. (b) Area A_{II}. (c) Area A_{III}. (d) Area A_{III}.

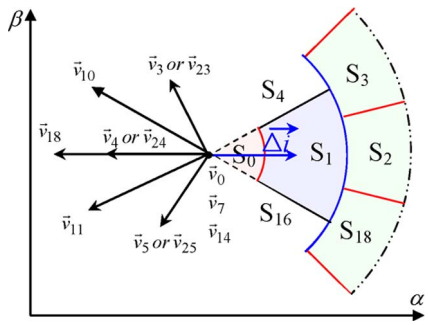

Fig. 8. Selection process of voltage vectors.

TABLE IV
NP CURRENT FOR SWITCHING COMBINATIONS OF DIFFERENT SMALL VECTORS

Small Vectors	i_{m2}	Sign of i_{m2}	C_1 charging state
$\vec{v}_1(100)$	$-i_{L1}$	-	discharge
$\vec{v}_{21}(0-1-1)$	i_{L1}	+	charge
$\vec{v}_2(110)$	i_{L3}	-	discharge
$\vec{v}_{22}(00-1)$	$-i_{L3}$	+	charge
$\vec{v}_3(010)$	$-i_{L2}$	-	discharge
$\vec{v}_{23}(-10-1)$	i_{L2}	+	charge
$\vec{v}_4(011)$	i_{L1}	-	discharge
$\vec{v}_{24}(-10\ 0)$	$-i_{L1}$	+	charge
$\vec{v}_5(001)$	$-i_{L3}$	-	discharge
$\vec{v}_{25}(-1-1\ 0)$	i_{L3}	+	charge
$\vec{v}_6(101)$	i_{L2}	-	discharge
$\vec{v}_{26}(0-10)$	$-i_{L2}$	+	charge

V. SIMULATION RESULTS

The presented simulation results are obtained with the following elements: $C_1 = C_2 = 7500\ \mu$F, $R = 30\ \Omega$, $L = 5$ mH, and $u_s = 350$ V; the hysteresis bands are $h_1 = 0$ A and $h_2 = 0.3$ A.

A. Simulation Waveforms of the SVCC

Fig. 10 shows the obtained simulation results with the applied SVCC. Fig. 10(a) and (b) clearly shows that the actual load current follows its reference. Fig. 10(c) shows the sector in which the error-vector tip is located. Fig. 10(d)–(f) displays the modulated voltage U_{10}, the phase-to-phase voltage U_{12}, and the line voltage v_{m1}, respectively. Fig. 10(g) shows the used voltage vectors of the three-phase NPC inverter in the $\alpha\beta$ frame. The current-error and the load-current trajectories in the $\alpha\beta$ frame are illustrated in Fig. 10(h) and (i), respectively.

The problem of NP unbalance can appear in sectors of area A_{III} when using only medium and large vectors. However, the error is always returned to the sectors of area A_{II} [Fig. 11(e)], so the switching redundancies can be used to balance the NP voltage.

In Fig. 11, the SVCC algorithm without NP voltage balancing is applied to the system before $t = 0.327$ s. As a result, the upper capacitor C_1 is discharging [Fig. 11(a)], and the lower capacitor C_2 is charging [Fig. 11(b)].

Therefore, the NP voltage unbalance affects directly the three-phase NPC inverter output voltages, as shown in Fig. 11(c). At $t = 0.376$ s, the NP voltage control is involved. Thus, the voltage across both capacitors u_{s1} and u_{s2} starts to converge toward the half of the dc voltage $u_s/2$.

In order to demonstrate the selection rule of the redundant inverter switching states, Fig. 11(d)–(f) shows, respectively,

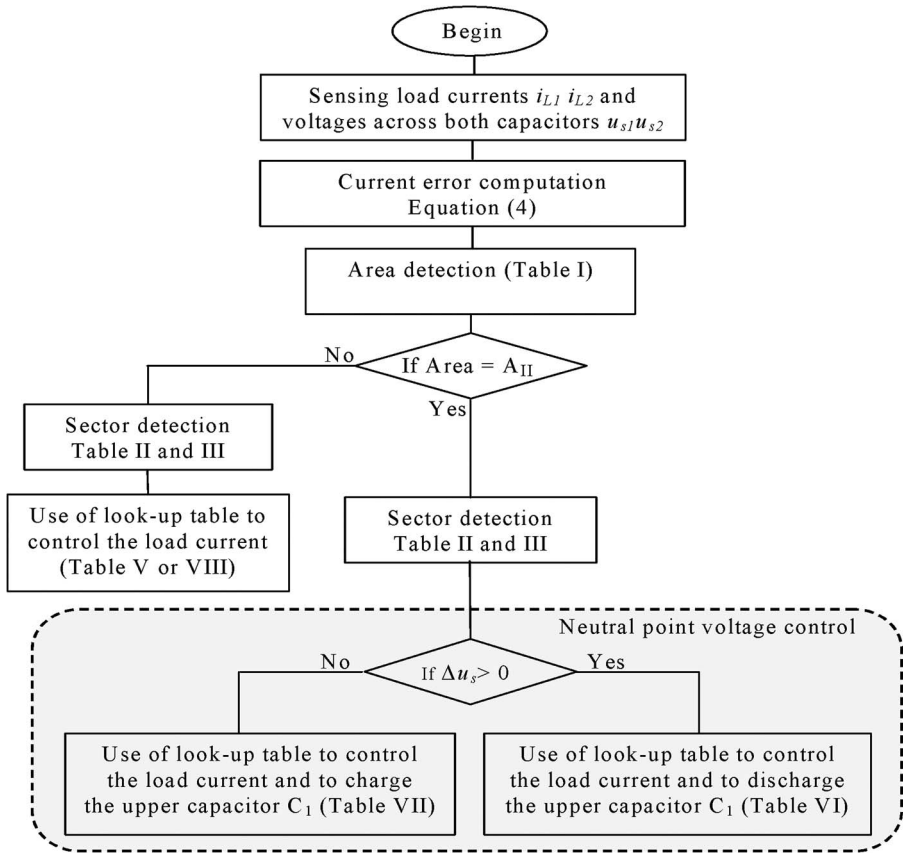

Fig. 9. The proposed SVCC algorithm with NP voltage control.

TABLE V
SWITCHING TABLE FOR AREA A_I

Area A_I	S_0
	$\vec{v}_0$ Or $\vec{v}_7$ Or $\vec{v}_{14}$

TABLE VI
SWITCHING TABLE FOR AREA A_{II} (C_1 DISCHARGING ACTION)

Area A_{II}	S_1	S_4	S_7	S_{10}	S_{13}	S_{16}
	$\vec{v}_4$	$\vec{v}_5$	$\vec{v}_6$	$\vec{v}_1$	$\vec{v}_2$	$\vec{v}_3$

TABLE VII
SWITCHING TABLE FOR AREA A_{II} (C_1 CHARGING ACTION)

Area A_{II}	S_1	S_4	S_7	S_{10}	S_{13}	S_{16}
	$\vec{v}_{24}$	$\vec{v}_{25}$	$\vec{v}_{26}$	$\vec{v}_{21}$	$\vec{v}_{22}$	$\vec{v}_{23}$

TABLE VIII
SWITCHING TABLE FOR AREA A_{III}

Area A_{III}	S_2	S_3	S_5	S_6	S_8	S_9
	$\vec{v}_{18}$	$\vec{v}_{11}$	$\vec{v}_{19}$	$\vec{v}_{12}$	$\vec{v}_{20}$	$\vec{v}_{13}$
	S_{11}	S_{12}	S_{14}	S_{15}	S_{17}	S_{18}
	$\vec{v}_{15}$	$\vec{v}_8$	$\vec{v}_{16}$	$\vec{v}_9$	$\vec{v}_{17}$	$\vec{v}_{10}$

the NP voltage ($\Delta u_s = u_{s1} - u_{s2}$), the area number, and the applied vector number during the short time interval $0.4044\ \text{s} < t < 0.4046$ s. For instance, at point A, Δu_s is negative [Fig. 11(d)], and the error-vector tip is located in area A_{II} [Fig. 11(e)]. Therefore, the positive switching state must be selected to increase the voltage across capacitor C_1. This is confirmed by the application of the voltage vector $\vec{v}_{24}$ as shown in Fig. 11(f). Similarly, at point B, where Δu_s is positive and the error-vector tip is still located in area A_{II}, vector $\vec{v}_4$ is applied to decrease the voltage across capacitor C_1.

B. Switching-Frequency Variation

The switching frequency may be calculated through the calculation of the switching number S_i during a time window $\Delta t = 0.1$ s and is given by

$$f = \frac{1}{2\Delta t} \sum_i S_i. \tag{7}$$

The simulation results in this section are given for both CHCC and SVCC strategies. The simulation parameters are the same for both methods. From Fig. 12(a), it can be seen that the switching frequency with the SVCC is lower than the one with the CHCC when the hysteresis bands h_1 and h_2 ($h_1 = h_2 = h$) vary.

The same consideration can be observed in Fig. 12(b) when the inductor of the load varies from 2.5 to 7.5 mH. In addition, the variation of the switching frequency for CHCC ($\Delta f = 28$ kHz) is larger than for SVCC ($\Delta f = 6$ kHz). These results confirm that the SVCC depends slightly on the load parameters. It can be noticed from Fig. 13(a) and (b) that the harmonic spectrum of the phase voltage (13.54%) obtained with SVCC

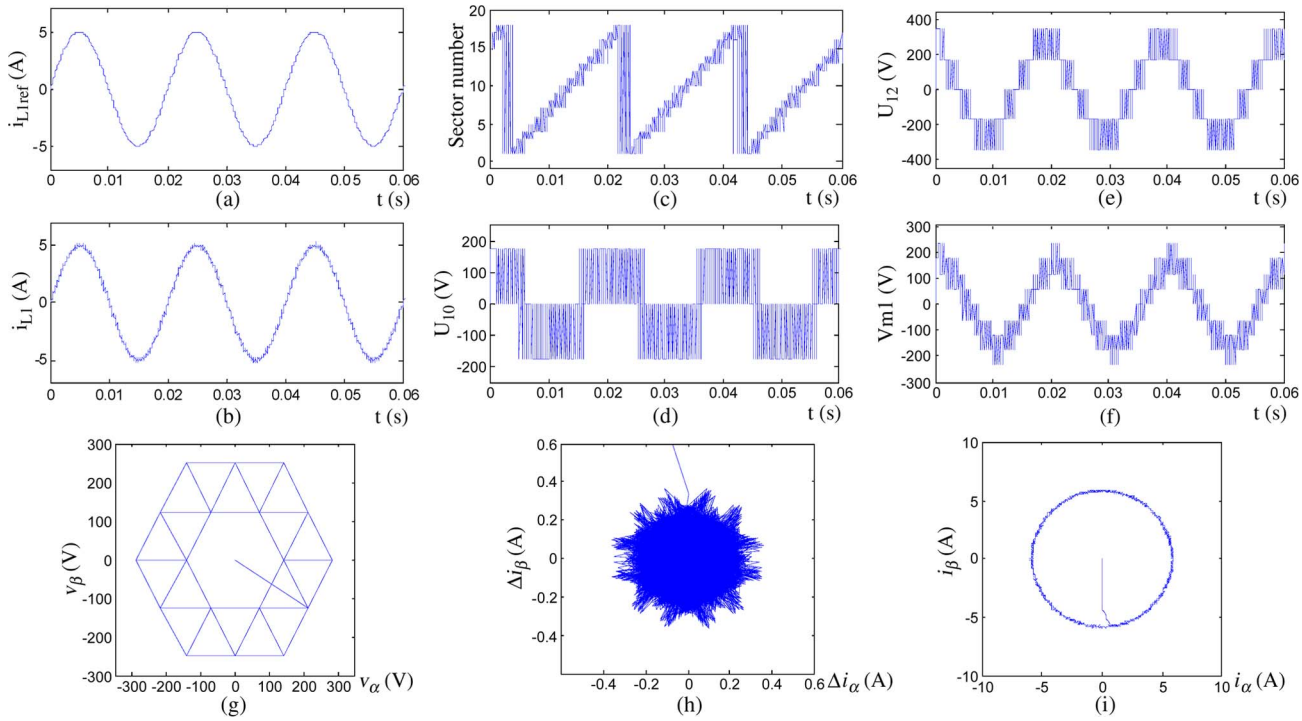

Fig. 10. Simulation waveforms of the SVCC applied on the three-phase NPC inverter. (a) Load current reference. (b) Load current. (c) Sector in which the error vector lies. (d) Modulated voltage U_{10}. (e) Phase-to-phase voltage U_{12}. (f) Line voltage v_{m1}. (g) Used voltage vectors of the three-phase NPC. (h) Current-error trajectory in the $\alpha\beta$ frame. (i) Load-current trajectory in the $\alpha\beta$ frame.

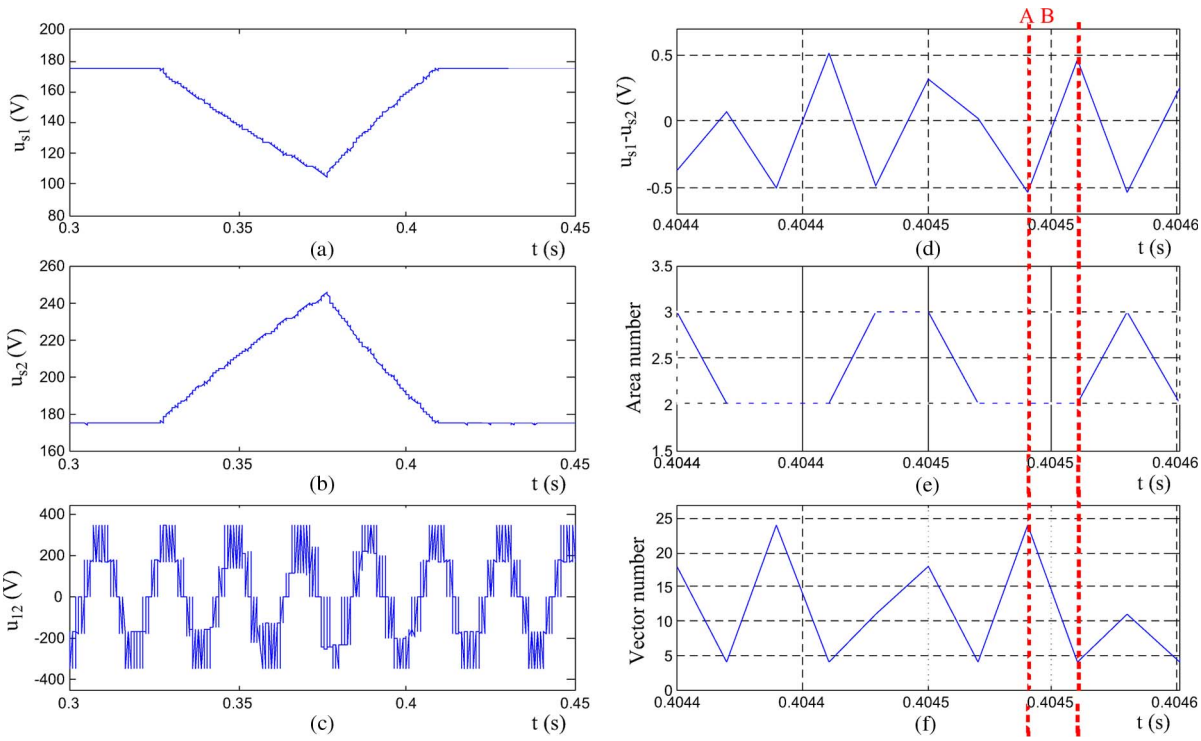

Fig. 11. Simulation waveforms of the NP voltage control. (a) Voltage across the upper capacitor C_1. (b) Voltage across the lower capacitor C_2. (c) Phase-to-phase voltage U_{12}. (d) NP voltage $U_{S1} - U_{S2}$. (e) Areas in which the error-vector tip lies. (f) Applied voltage vector.

is smaller than the harmonic spectrum of the phase voltage (22.8%) obtained with CHCC. This is due to the regularity of the commutations along the fundamental period and the use of the adjacent voltage vectors by the SVCC strategy.

C. Switching Regularity

Fig. 14(a) and (b) shows the gate drive signal for the first switch of the inverter T_{11} with the CHCC and the SVCC methods, respectively.

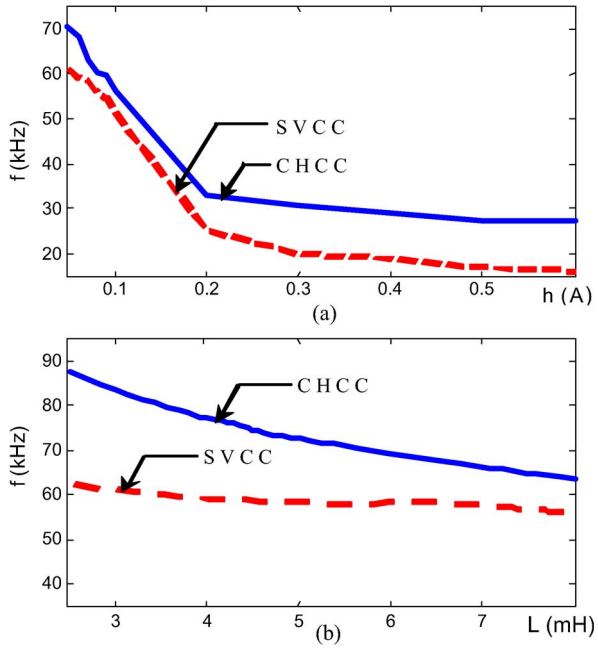

Fig. 12. Switching-frequency variation for both CHCC and SVCC methods. (a) Switching-frequency variation versus hysteresis band. (b) Switching-frequency variation versus inductor value.

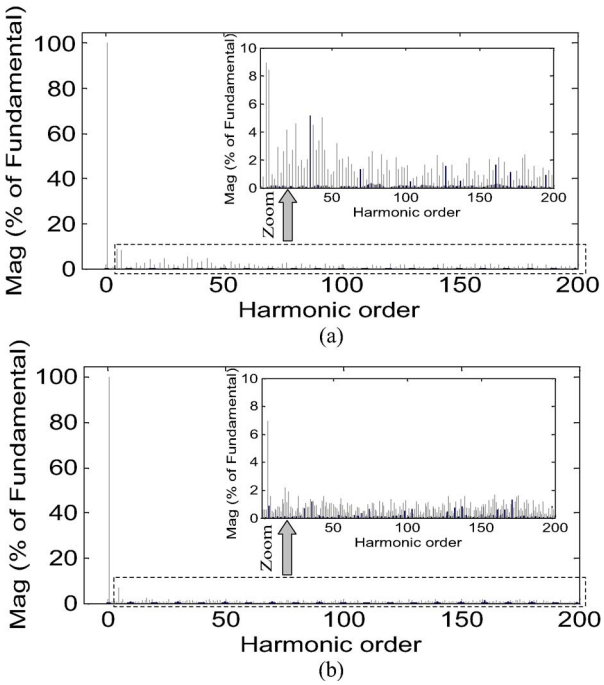

Fig. 13. Harmonic spectrum for both CHCC and SVCC methods. (a) Harmonic spectrum of the phase voltage given by CHCC. (b) Harmonic spectrum of the phase voltage given by SVCC.

For the SVCC, the switching occurs for the majority of the input current waveform, while for the CHCC, there are times in which no switching occurs $(0.0249\ \text{s} < t < 0.0256\ \text{s})$ due to the interaction of the phases. It can be observed from the gate drive signal that there is no switching occurring at the peak of the fundamental current for CHCC [Fig. 14(a)] while for SVCC, more regular switching occurs [Fig. 14(b)]. This can be explained by the fact that the SVCC gathers the three current

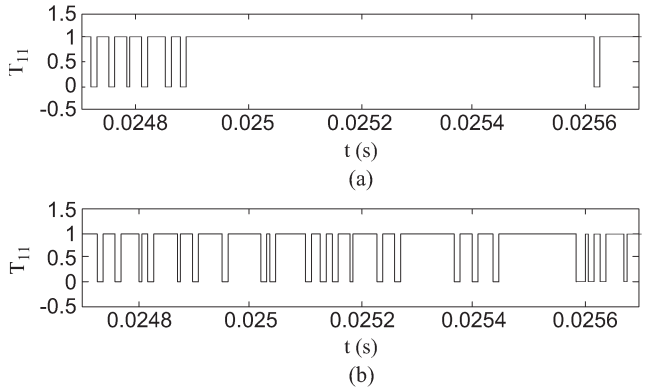

Fig. 14. Gate signal for the first switch of the inverter with both CHCC and SVCC methods. (a) With the CHCC method. (b) With the SVCC method.

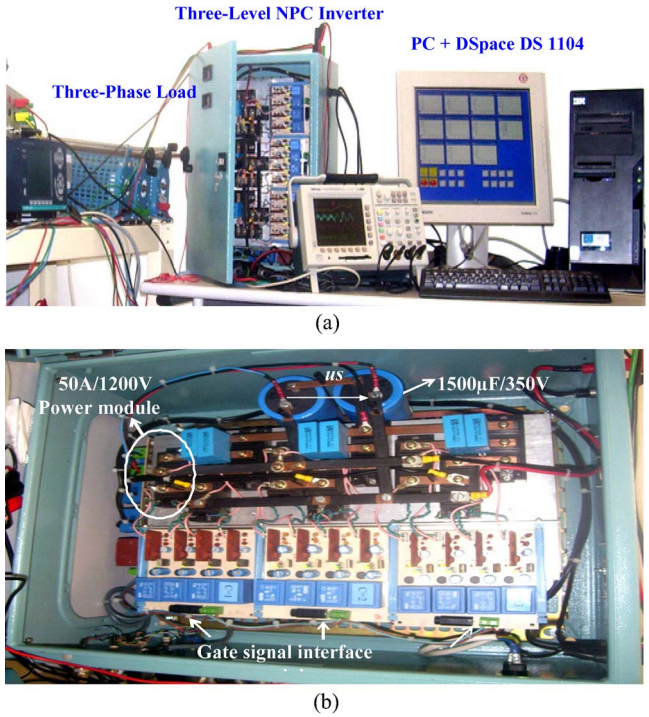

Fig. 15. Experimental system. (a) Experimental setup. (b) NPC prototype.

errors into one single vector, and hence, there is no interaction between the phases.

VI. Experimental Results

Fig. 15(a) shows the built experimental system. The overall current-control technique (shown in Fig. 4) is implemented on the DS1104 DSPACE board, which is plugged into a PC. Fig. 15(b) shows the used NPC prototype for our experimental validations. The power components are designed for a 6-kVA operating drive 400-V 50-Hz ac, and the rectifier yields a constant full dc voltage $us = 170$ V. The power modules are two bridged insulated-gate bipolar transistors that have been packed into one module. 1500-μF/350 V capacitors, a 5-mH self- and 30-Ω resistances are used. Current and voltage measurements are sensed using Hall-effect sensors and then injected into the analog-to-digital converter of the DS1104 DSPACE board.

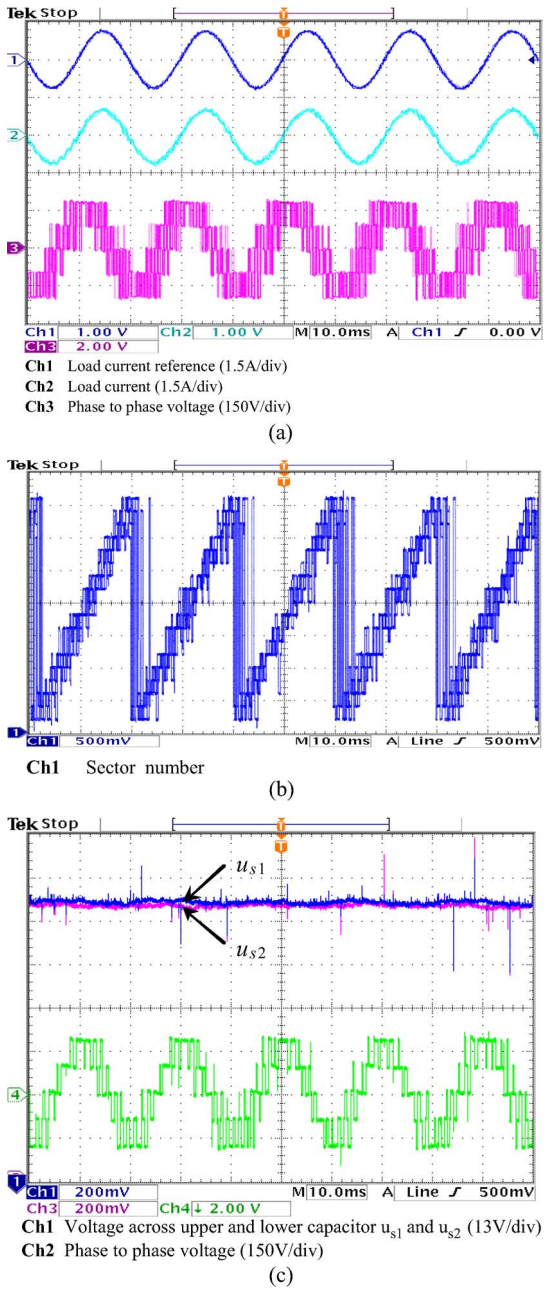

Fig. 16. Experimental results of the three-phase three-level NPC inverter controlled by the proposed SVCC during the steady state.

Fig. 16 shows the experimental waveforms obtained for the three-phase NPC inverter controlled by the proposed SVCC. Fig. 16(a) shows that the load current follows its reference within the hysteresis boundary areas. From Fig. 16(b), it is clearly shown that the error current moves in the eighteen possible sectors (except for sector S_0 since h_1 is taken equal to zero).

Fig. 16(c) shows that the u_{s1} and u_{s2} voltages across the upper and the lower capacitors are equal. Therefore, the NP voltage is well controlled by using the redundant inverter switching states.

Fig. 17(a) and (b) shows the waveform of the load-current reference, the load current, and the phase-to-phase voltage in case of a step change in magnitude and frequency of the load-current reference. It is clear that the results confirm the validity of the proposed method even in the case of transient states.

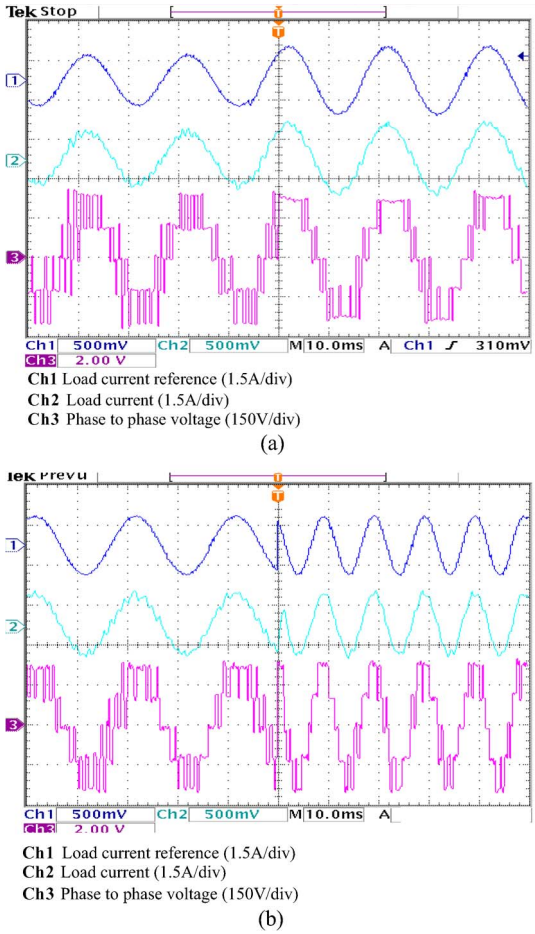

Fig. 17. (a) Experimental results with a step change in the magnitude of the load-current reference. (b) Experimental results with a step change in the frequency of the load-current reference.

VII. Conclusion

This paper has presented a control of the three-phase NPC inverter by means of an SVCC that uses circular hysteresis areas.

The three current errors are gathered into a single space-vector quantity that can be located in 19 sectors. Consequently, the line-current interactions are avoided in the three-phase system. The number and the position of the current-error sectors, in which the error vector moves, have been chosen in order to ensure the switching between two adjacent voltage levels of the inverter. The selection of the appropriate voltage vector is based on forcing the actual load current to follow the reference load current and also to control the NP voltage owing to the use of the redundant inverter switching states. The original strategy has been detailed for the three-level NPC structure and can be extended to a five-level one [26]–[28]. The definition of the three circular hysteresis bands around the error vector has been implemented in real time on an NPC inverter. The proposed selection process of the next applied vector and the minimization of the error vector have been verified through simulations and experimental tests. The switching frequency is decreased, and a more regular switching is obtained

comparatively with the conventional hysteresis while retaining its robustness. In addition, the proposed scheme can be adapted to other multilevel inverter structures.

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